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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/075,043	02/12/2002	David Tseng	56956 (71987)	56956 (71987) 7505	
21874	7590 03/17/2004		EXAM	EXAMINER	
EDWARDS & ANGELL, LLP			NGUYEN, KHIEM D		
P.O. BOX 55874 BOSTON, MA 02205			ART UNIT	PAPER NUMBER	
200101., 1			2823	-	
			DATE MAILED: 03/17/200-	DATE MAILED: 03/17/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

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<del>- : · · · · · · · · · · · · · · · · · · </del>		Application No.	Applicant(s)	
		10/075,043	TSENG ET AL.	
	Office Action Summary	Examiner	Art Unit	
:		Khiem D Nguyen	2823	
Period f	The MAILING DATE of this communication app or Reply	pears on the cover sheet with	the correspondence addres	:s
THE - Extended - aftended - if thended - if Noinend - Fail - Any	HORTENED STATUTORY PERIOD FOR REPL' MAILING DATE OF THIS COMMUNICATION. ensions of time may be available under the provisions of 37 CFR 1.1 r SIX (6) MONTHS from the mailing date of this communication. e period for reply specified above is less than thirty (30) days, a reply D period for reply is specified above, the maximum statutory period v ure to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing led patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply y within the statutory minimum of thirty (3 will apply and will expire SIX (6) MONTH , cause the application to become ABAN	y be timely filed 30) days will be considered timely. S from the mailing date of this commu DONED (35 U.S.C. § 133).	nication.
1)🖂	Responsive to communication(s) filed on 24 I	December 2003 .		
2a)□	This action is <b>FINAL</b> . 2b)⊠ Th	is action is non-final.		
3) <u></u>	Since this application is in condition for allowation of closed in accordance with the practice under			erits is
: · _	tion of Claims			
: 4)\(\times\)	Claim(s) <u>1-41</u> is/are pending in the application			
·	4a) Of the above claim(s) is/are withdraw	wh from consideration.		
· 5)∐	Claim(s) is/are allowed.			
6)[	. ,			
7)∐	Claim(s) is/are objected to.			
	Claim(s) are subject to restriction and/o tion Papers	r election requirement.		
9)	The specification is objected to by the Examine	er.		
10)🛛	The drawing(s) filed on 12 February 2002 is/are	e: a)⊠ accepted or b)⊡ object	ted to by the Examiner.	
	Applicant may not request that any objection to th	e drawing(s) be held in abeyand	ce. See 37 CFR 1.85(a).	
11)	The proposed drawing correction filed on	_ is: a)□ approved b)□ disa	approved by the Examiner.	
	If approved, corrected drawings are required in re	ply to this Office action.		
12)	The oath or declaration is objected to by the Ex	aminer.		
Priority	under 35 U.S.C. §§ 119 and 120			
∃13)⊠	Acknowledgment is made of a claim for foreign	n priority under 35 U.S.C. § 1	19(a)-(d) or (f).	
a	⊠ All b)□ Some * c)□ None of:			
:	1.⊠ Certified copies of the priority document	s have been received.		
:	2. Certified copies of the priority document	s have been received in App	lication No	
*	3. Copies of the certified copies of the prio application from the International Bu See the attached detailed Office action for a list	reau (PCT Rule 17.2(a)).		ge
14)	Acknowledgment is made of a claim for domesti	ic priority under 35 U.S.C. §	119(e) (to a provisional app	olication).
:	a) $\square$ The translation of the foreign language pro Acknowledgment is made of a claim for domest			
Attachme	_			
2) 🔲 Noti	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449) Paper No(s)	· —	mmary (PTO-413) Paper No(s) ormal Patent Application (PTO-15.	

Art Unit: 2823

#### **DETAILED ACTION**

## Response to Amendment

The non-final rejection as set forth in paper No. (4) is withdrawn in response to applicants' amendments. A new rejection is made as set forth in this Office Action.

Claims (1-41) are pending in the application.

# Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 1. Claims 1-21 and 33-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al. (U.S. Patent 6,117,693).

In re claims 1, 12, and 33, Fogal discloses a wire bonding method for use in fabrication of a semiconductor package, comprising the steps of (col. 3, line 17 to col. 6, line 38 and FIGS. 1-6): (1) preparing a substrate (FIG. 4: 10) composed of a plurality of substrate units, and mounting at least a chip (FIG. 4: 12) on each of the substrate units; (2) providing a wire bonding station (FIG. 6: 70) at least having a wire bonding mechanism and a testing mechanism (FIG. 6: 24) so as to allow the substrate mounted with the chips to be introduced into the wire bonding mechanism; (3) forming a plurality of bonding wires (FIG. 4: 32) on one substrate unit of the substrate via the wire bonding mechanism so as to electrically connect a corresponding chip to the substrate unit; (4) introducing the wire-bonded substrate unit into the testing mechanism for performing an

Art Unit: 2823

O/S (open/short) test (col. 4, line 64 to col. 5, line 2 and FIG. 1), and forming bonding wires on a next adjacent substrate of the substrate simultaneously moved into the wiring bonding mechanism (col. 6, lines 7-8-27); wherein if test results indicate no occurrence of wire opening or short circuit for the bonding wires formed on the wire-bonded substrate unit, then step (5) proceeds (col. 2, lines 29-51 and FIG. 1); wherein if the test results indicate occurrence of wire opening or short circuit for the bonding wires on the wire-bonded substrate unit, the testing mechanism is prompted to generate a control signal to the wire bonding mechanism for interrupting a wire bonding process, whereby the wire bonding mechanism is adjusted or repaired (col. 2, lines 29-38), or other causes of wire opening or short circuit are traced and overcome, so as to rework the bonding wires on the wire-bonded substrate united, and then repeat the step (4); (5) repeating the step (3) until all the substrate units of the substrate are wire-bonded and tested with the O/S test, and then proceeding with step (6); and (6) moving the wire-bonded and tested substrate out of the wire bonding station, for allowing the substrate to be used in subsequent package fabrication (col. 2, lines 38-51).

In re claims 2, 13, and 34, <u>Fogal</u> discloses wherein the testing mechanism includes at least a test socket and a tester electrically connected to the test socket (FIG. 6).

In re claims 3, 14, and 35, <u>Fogal</u> discloses wherein the test socket is used to come into contact with the wire-bonded substrate unit, allowing the tester (FIG. 6: 24) to perform the O/S test for the bonding wires on the substrate unit through the test socket (col. 4, line 64 to col. 5, line 2).

Art Unit: 2823

In re claims 4, 15, 36, and 38, <u>Fogal</u> discloses wherein the tester (FIG. 6: 24) at least includes: a testing module electrically connected to the test socket, for performing the O/S test through the test socket (col. 4, line 64 to col. 5, line 2); and a controlling module electrically connected to the testing module and the wire bonding mechanism for receiving a test-failure signal from the testing module in occurrence of wire opening or short circuit, generating a control signal to the wire bonding mechanism (FIG. 6: 70) so as to interrupt the wire bonding process in the wire bonding mechanism; and a displaying module connected to the testing module, for displaying test results from the test module (col. 6, lines 18-38).

In re claims 5, 16, and 39, **Fogal** discloses wherein the tester is further electrically connected to a test socket of at least another wire bonding station so as to simultaneously control test sockets in a plurality of wire bonding, so as to simultaneously control test sockets in a plurality of wire bonding stations for performing the O/S test (col. 6, lines 18-38 and **FIGS. 1 and 6**).

In re claims 6 and 17, <u>Fogal</u> discloses wherein the wire bonding station further includes a handling mechanism for moving the substrate into or out of the wire bonding station (col. 6, lines 18-38 and FIG. 6).

In re claims 7 and 18, **Fogal** discloses wherein the wire bonding station is a wire bonding machine internally provided with the testing mechanism and the testing mechanism is disposed at a downstream position relative to the wire bonding mechanism in the wire bonding machine (**FIG. 6**).

Art Unit: 2823

In re claims 8 and 19, <u>Fogal</u> discloses wherein the wire bonding station includes a wire bonding machine internally provided with at least a test socket, and a tester (FIG. 6: 24) externally connected to the wire bonding machine (FIG. 6: 70) and electrically connected to the test socket, which test socket is disposed at a downstream position relative to the wire bonding mechanism.

In re claims 9 and 37, <u>Fogal</u> discloses wherein the step (4), upon receiving the control signal from the testing mechanism the wire bonding mechanism interrupts the wire bonding process after the next adjacent substrate unit is completely wire-bonded (col. 6, lines 18-38).

In re claims 10, 20, and 40, <u>Fogal</u> discloses wherein the substrate units of the substrate are arranged in a matrix type (FIGS. 1, 2, and 6).

In re claims 11, 21, and 41, <u>Fogal</u> discloses wherein the substrate units of the substrate are arranged in a single-array type (FIGS. 1, 2, and 6).

2. Claims 22-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al. (U.S. Patent 6,117,693).

In re claim 22, <u>Fogal</u> discloses a wire bonding method for use in fabrication of a semiconductor package, comprising the steps of (col. 3, line 17 to col. 6, line 38 and FIGS. 1-6): (1) preparing a substrate (FIG. 4: 10) composed of a plurality of substrate units, and mounting at least a chip (FIG. 4: 12) on each of the substrate units; (2) providing a wire bonding station (FIG. 6: 70) at least having a wire bonding mechanism and a testing mechanism (FIG. 6: 24) so as to allow the substrate mounted with the chips to be introduced into the wire bonding mechanism; (3) forming a plurality of bonding

Art Unit: 2823

wires (FIG. 4: 32) on one substrate unit of the substrate via the wire bonding mechanism so as to electrically connect a corresponding chip to the substrate unit; (4) introducing the wire-bonded substrate unit into the testing mechanism for performing an O/S (open/short) test (col. 4, line 64 to col. 5, line 2 and FIG. 1), and forming bonding wires on a next adjacent substrate of the substrate simultaneously moved into the wiring bonding mechanism (col. 6, lines 7-27); (5) proceeding with step (7) if test result indicate no occurrence of wire opening or short circuit for the bonding wires formed on the wirebonded substrate unit (col. 5, lines 47-60); wherein, if no wire opening or short circuit occurs, or else, a controlling module of the testing mechanism determining if a preinputted command to the testing mechanism is to interrupt a wiring bonding process in the wire bonding mechanism; wherein, the pre-inputted command interruption of the wire bonding process, then step (6) proceeds; or else, step (9) proceeds; (6) generating a control signal via the controlling module of the testing mechanism to the wire bonding mechanism for interrupting the wire bonding process, so as to trace and overcome causes of wire opening or short circuit, and to rework the wire-bonded substrate unit (col. 6, lines 18-38); then repeating the step (4); (7) repeating the step (3) until all the substrate units of the substrate are wire-bonded and tested with the O/S test, and then proceeding with step (8) (FIG. 1); (8) moving the wire-bonded and tested substrate out of the wire bonding station, for allowing the substrate to be used in subsequent package fabrication (col. 5, lines col. 5, lines 47-60); (9) displaying test results produced from the step (5) via a displaying module of the testing mechanism, and repeating the step (3) until all the substrate units of the substrate are wire-bonded and tested with the O/S test; then

Art Unit: 2823

proceeding with step (10); (10) moving the wire-bonded and tested substrate out of the wire bonding station; and (11) reworking wire-opened or short-circuited substrate units, and tracing and overcoming causes of wire opening or short circuit according to the displayed test results by the displaying module of the testing mechanism (col. 6, lines 18-38).

In re claim 23, <u>Fogal</u> discloses wherein the testing mechanism includes at least a test socket and a tester electrically connected to the test socket (FIG. 6).

In re claim 24, <u>Fogal</u> discloses wherein the test socket is used to come into contact with the wire-bonded substrate unit, allowing the tester (FIG. 6: 24) to perform the O/S test for the bonding wires on the substrate unit through the test socket (col. 4, line 64 to col. 5, line 2).

In re claim 25, <u>Fogal</u> discloses wherein the tester (FIG. 6: 24) at least includes the controlling module, the displaying module and a testing module, the testing module being electrically connected to the test socket so as to perform the O/S test for the substrate unit through the test socket (col. 4, line 64 to col. 5, line 2); and transmit test results to the controlling module and the displaying module (col. 6, lines 18-38)

In re claim 26, <u>Fogal</u> discloses wherein the tester is further electrically connected to a test socket of at least another wire bonding station so as to simultaneously control test sockets in a plurality of wire bonding, so as to simultaneously control test sockets in a plurality of wire bonding stations for performing the O/S test (col. 6, lines 18-38 and FIGS. 1 and 6).

Page 8

Application/Control Number: 10/075,043

Art Unit: 2823

In re claim 27, **Fogal** discloses wherein the wire bonding station further includes a handling mechanism for moving the substrate into or out of the wire bonding station (col. 6, lines 18-38 and **FIG. 6**).

In re claim 28, <u>Fogal</u> discloses wherein the wire bonding station is a wire bonding machine internally provided with the testing mechanism and the testing mechanism is disposed at a downstream position relative to the wire bonding mechanism in the wire bonding machine (FIG. 6).

In re claim 29, <u>Fogal</u> discloses wherein the wire bonding station includes a wire bonding machine internally provided with at least a test socket, and a tester (FIG. 6: 24) externally connected to the wire bonding machine (FIG. 6: 70) and electrically connected to the test socket, which test socket is disposed at a downstream position relative to the wire bonding mechanism.

In re claim 30, <u>Fogal</u> discloses wherein the step (6), upon receiving the control signal from the testing mechanism the wire bonding mechanism interrupts the wire bonding process after the next adjacent substrate unit is completely wire-bonded (col. 6, lines 18-38).

In re claim 31, <u>Fogal</u> discloses wherein the substrate units of the substrate are arranged in a matrix type (FIGS. 1, 2, and 6).

In re claims 32, <u>Fogal</u> discloses wherein the substrate units of the substrate are arranged in a single-array type (FIGS. 1, 2, and 6).

Art Unit: 2823

## Response to Amendment

## Response to Arguments

3. In response to Applicants' argument that Bertolet and AAPA whether taken alone or in combination, fail to teach or suggest performing an open/short (O/S) test on one substrate unit while wire bonding a next adjacent substrate unit in the wire bonding station.
Moreover, there is no teaching or suggestion of providing a wire bonding station having at least a wire bonding mechanism and a testing mechanism that are capable of performing an O/S test on one substrate unit of a substrate while simultaneously wirebonding the next adjacent substrate unit, examiner respectfully disagree. Applicants are directed to the pages 2 and 3 presented in this Office Action where the newly discovered reference Fogal et al. (U.S. Patent 6,117,693) disclosed the above cited claim limitations.

### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Art Unit: 2823

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N. March 10, 2004

> W. DAVID COLEMAN PRIMARY EXAMINER